REMARKS

Claims 1-29 are pending in the present application. Claims 1 and 16 have been amended. No new matter has been added.

Claims 1, 4-8, and 16-19 have been rejected under 35 U.S.C. § 102(a) as assertedly being anticipated by U.S. Patent No. 6,456,335 B1 to Kunikiyo (hereinafter "Kunikiyo"). Claims 2, 3, 8, 9, 20, 21, 23, and 24 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Kunikiyo. Claims 10-15, 22, and 25-29 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Kunikiyo in view of U.S. Patent No. 6,417,056 B1 to Quek et al. (hereinafter "Quek"). Applicants respectfully traverse these rejections.

Regarding claim 1, Applicants claim 1 recites at least one distinguishing feature of the present invention, namely the steps of "oxidizing the wafer creating an oxidized layer *prior to* removing the mask layer" and "removing the oxidized layer and the mask layer positioned over the structure." In other words, an oxidized layer is formed before the mask layer is removed and, a*fter the* oxidized layer is formed, the mask layer and the oxidized layer positioned over the structure are removed. The cited references fail to disclose these steps.

The Office Action cited Kunikiyo, column 9, lines 55-65 and column 9, lines 60-65 as disclosing these steps, respectively. The cited section is provided below for reference.

> In this specification, this step is referred to as "re-oxidation of the gate". The oxidizing atmosphere may be any of a dry O_2 atmosphere, a wet O_2 atmosphere, an HCl/O_2 atmosphere, an NO atmosphere, an N_2O atmosphere and an N_2 /dry O_2 atmosphere. Thus, etching damages caused on the upper surface of the silicon substrate 1 or the side surfaces of the gate structure 91 in the anisotropic dry etching steps for forming the gate structure 91 can be captured in an oxide film formed by the thermal oxidation. Further, crystal defects caused in the ion implantation steps for forming the extensions 19 and the pocket implantation layers 20 can be recovered.

(Kunikiyo, column 9, lines 55-65.)

Notably, this section of Kunikiyo fails to disclose the step of "oxidizing the wafer creating an oxidized layer *prior to* removing the mask layer" and "*removing* the oxidized layer

and the *mask layer* positioned over the structure" as recited in Applicants claim 1. It should be noted that the insulator layer 12 is utilized as a mask in Kunikiyo (see Figures 7 and 8) and that the mask (insulator layer 12) is not removed (see Figure 21).

Thus, because Kunikiyo fails to disclose at least one limitation of Applicants' claim 1, claim 1 is deemed to be in condition for allowance. Claims 2-15 depend from and further limit independent claim 1 in a patentable sense and, therefore, are also deemed to be in condition for allowance. Accordingly, it is respectfully requested that the rejections of claims 1-15 be reconsidered and withdrawn.

Regarding claim 16, Applicants claim 16 recites at least one distinguishing feature of the present invention, namely the steps of "oxidizing the wafer creating an oxidized layer *prior to* removing the mask layer" and "*removing the mask layer* and the oxidized layer over remaining portions of the polysilicon layer." In other words, an oxidized layer is formed *before* the mask layer is removed and, *after the* oxidized layer is formed, the mask layer and the oxidized layer are removed over remaining portions of the polysilicon layer. The cited references fail to disclose these steps.

The Office Action cited Kunikiyo, column 10, lines 15-20 and column 10, lines 45-60 as disclosing these steps, respectively. Each of the cited sections are provided below for reference.

> Then, RTO (rapid thermal oxidation) is performed in a dry O_2 atmosphere or a wet O_2 atmosphere. Consequently, the insulator films 21 consisting of nitride films are oxidized to form an insulator film 22 consisting of an oxynitride film (FIG. 11).

(Kunikiyo, column 10, lines 15-20.)

> Then, a prescribed insulator film such as a silicon oxide film, a silicon nitride film or a silicon oxynitride film (or a multilayer film of such films) is formed on the overall surface to cover the insulator film 22, and the aforementioned prescribed insulator film is thereafter etched by anisotropic dry etching at a high etching rate along the depth direction of the silicon substrate 1, thereby forming side walls 23. The side walls 23 are formed on the side surfaces of the gate structure 91 in a self-aligned manner. In the insulator film 22 formed on the upper surface of the silicon substrate 1, parts not serving as underlayers for the side walls 23 are removed through the anisotropic dry etching for forming the side walls 23, to expose the upper surface of the silicon substrate 1 (FIG.

12).

> Then, an impurity is introduced into the upper surface of the silicon substrate 1 by ion implantation through the gate structure 91 and the side walls 23 serving as implantation masks and heat treatment is thereafter performed thereby forming source/drain regions 24 to be deeper than the pocket implantation layers 20 in a self-aligned manner.

(Kunikiyo, column 10, lines 44-63.)

Notably, this section of Kunikiyo fails to disclose the steps of "oxidizing the wafer creating an oxidized layer *prior to* removing the mask layer" and "*removing the mask layer* and the oxidized layer over remaining portions of the polysilicon layer." as recited in Applicants claim 16. It should be noted that the insulator layer 12 is utilized as a mask in Kunikiyo (see Figures 7 and 8) and that the mask (insulator layer 12) is not removed (see Figure 21). It should also be noted that the phrase "the insulator film" etched at column 10, line 48 (". . . and the aforementioned prescribed insulator film is thereafter etched . . .") is not referring to the mask 12 of FIG. 12. Rather, the phrase "the insulator film" is referring to the layer deposited to form the spacers 23 of FIG. 12, as evidenced by the phrase "thereby forming side walls 23." (Kunikiyo, column 10, lines 44-51.)

Thus, because Kunikiyo fails to disclose at least one limitation of Applicants' claim 16, claim 16 is deemed to be in condition for allowance. Claims 17-29 depend from and further limit independent claim 16 in a patentable sense and, therefore, are also deemed to be in condition for allowance. Accordingly, it is respectfully requested that the rejections of claims 16-29 be reconsidered and withdrawn.

In view of the above, Applicants respectfully submit that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicants request that the Examiner contact Applicants' attorney at the address below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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